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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/765,377
Filing Date: January 27, 2004
Appellant(s): PAYNE ET AL.

Alan K. Stewart
For Appellant

EXAMINER'S ANSWER

This is in response to the supplemental appeal brief filed 10/4/2007 appealing from the Office action mailed 11/14/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4,253,163	Komoriya et al.	02-1981
5,508,644	Branson et al.	04-1996
US2002/0171453	Kanamori et al.	11-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Komoriya et al. (USP 4,253,163).

Figure 1 shows a sense amplifier comprising a regenerative latch (T9, T10), an input differential pair of transistors (T1, T2) coupled to the regenerative latch, a leakage device (T13) coupled to each of the transistors comprising the input differential pair of transistors, said leakage device adapted to maintain the input differential pair of transistors in an on state during a precharge phase, and wherein the regenerative latch comprises a first transistor (18), second transistor (T5) and a third transistor (T6) and a clock signal node (18) as called for in claims 1-2.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Branson et al. (USP 5,508,644) in view of Kanamori et al. (US 2002/0171453).

Figure 1 of Branson et al. shows a sense amplifier comprising a regenerative latch (12, 14, 16, 18), an input differential pair of transistors (20, 22) coupled to the regenerative latch, a leakage device (26) coupled to each of the transistors comprising the input differential pair of transistors, said leakage device adapted to maintain the input differential pair of transistors in an on state during a precharge phase, and wherein the regenerative latch comprises a second transistor (34) and a third transistor (36) and a clock signal node (LE).

Branson et al. does not show a third transistor coupled in between the input differential transistor as called for in claims 1-2. Kanamori et al. show a sense amplifier including a transistor coupled in between of the differential input transistors to maintain an equal potential between the differential transistors thus minimizing erroneous operation. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to include a transistor in between the differential input transistors (20, 22) of Branson et al. for the purpose of maintaining an equal potential between the differential transistors thus minimizing erroneous operation.

(10) Response to Argument

35USC 102(b) as being anticipated by Komoriya et al. (USP 4,253,163):

Regarding the rejection of claims 1-2 as being anticipated by Komoriya et al., appellant argues that Komoriya et al. does not teach "a leakage device coupled to each of the transistors comprising the input differential pair of transistors, said leakage device adapted to maintain the input differential pair of transistors in an on state during a precharge phase" is not persuasive. Figure 1 of Komoriya et al. shows the leakage device (13) coupled to each of the transistors (T1 and T2) via transistors T5 and T6. During a pre-charge phase, i.e., the signal at terminal 18 is at

Vcc level, the transistors T5, T6 and T8 are on providing a current along paths T1, T5, T13; T2, T6, T13 thus anticipates the limitation of maintaining the input differential pair of transistors in an on state during a precharge phase as called for in claim 1. Therefore, the limitations of claims 1-2 are fully anticipated by Komoriya et al. reference.

35USC 103(a) as being unpatentable over Branson et al. (USP 5,508,644) in view of Kanamori et al. (US 2002/0171453):

Regarding the rejection of claims 1-2 under 103(a) as being unpatentable over Branson et al. (USP 5,508,644) in view of Kanamori et al. (US 2002/0171453), appellant argues that combined references does not teach "the regenerative latch comprises a first transistor coupled between the pair of transistors, a second transistor coupled to a first one of the pair of transistors and a third transistor coupled to a second one of the pair of transistors, wherein the first, second and third transistors are controlled by a clock signal node" as called for in claim 1 is not persuasive. Figure 1 of Branson et al. shows first and second transistors (34, 36) coupled to the same clock signal (LE). Branson et al. does not show a third transistor coupled to the pair of input transistors for receiving the same clock signal. Kanamori et al. shows a differential amplifier comprising a regenerative latch in which the first, second and third transistors (110, 120 and 140) receiving the clock signal (CK). The third transistor is used to maintain an equal potential between the pair of the input transistors. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to include a third transistor receiving the same clock signal (LE) in between the pair of the input transistors of Branson et al. for the purpose of maintaining an equal potential between the pair of the input transistors thus minimizing erroneous operation.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Conferees:

Timothy P. Callahan, SPE.

Ricky Mack, SPE.

Tuan T. Lam, Primary Examiner.